An Electrical Fan-Out Wafer Level Packaging Test Vehicle and Update on the Advanced System Integration Program

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Abstract

The on-going advance of microelectronic based activity, including mobile devices, edge computing, connected sensors and cloud-based operations, is driving the semiconductor industry to come up with faster devices and smaller form factors. The traditional route to CMOS miniaturization via device level scaling is reaching its limit. The need for next generation smart sensors and other advanced devices is steering the semiconductor industry to look at the integration of materials beyond silicon. To address these challenges, the advanced system integration program at BRIDG is aimed at developing solutions through innovative technologies aimed at package level scaling and heterogeneous integration on a conventional silicon platform.

The Ultra High Density Interposer project is a multi-year activity focused on developing stacked interposers with signal input/output (I/O) an order of magnitude higher than typically achieved. In this phase, a multi-chip daisy chain circuit is defined that will allow testing via continuity, humidity, and thermal cycling to demonstrate the integrity of the interconnect layers, underfill and overmold. An overview of the design and initial process integration results will be presented. A status overview of the advanced integration program being pursued at BRIDG will also be provided.